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Electronic Ballast Using a Symmetrical Half-bridge Inverter Operating at Unity-Power-factor and High Efficiency

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ABSTRACT

This paper deals with novel electronic ballast based on single-stage power processing topology using a symmetrical half-bridge inverter and current injection circuit. The half-bridge inverter drives the output parallel resonant circuit and injects current through the power factor correction (PFC) circuit. Because of high frequency current injection and high frequency modulated voltage, the proposed circuit maintains the unity power factor (UPF) with low THD even under wide variation in ac input voltage. This circuit needs minimum and lower sized components to achieve the UPF and high efficiency. This leads to an increase in reliability of ballast at low cost. Furthermore, to reduce cost, the electronic ballast is designed for two series-connected fluorescent lamps (FL). The analysis and experimental results are presented for (2 x 36 Watt) fluorescent lamps operating at 50 kHz switching frequency and input line voltage (230 V, 50 Hz).

Keywords: Zero-voltage-switching, unity power factor, power factor correction

1. Introduction

In recently reported single-stage electronic ballasts [1-3], the dc-bus voltage is maintained above the double value of peak input ac voltage as in two-stage ballast [4]. Whereas, the electronic ballast circuit in [5] maintains the dc-bus voltage only above the peak of input ac voltage. These single-stage ballasts are most suitable for low utility voltage up to 110 V. They have unequal switch voltages and switch currents in a switching cycle and will have high switch voltage stress in case of utility voltage above 110 V. The dimmable ballast proposed in [6] uses three switches. A simple, single-switch, high power factor electronic ballast given in [7] is based on a flyback push-pull converter, in which the line voltage is not necessarily lower than the output voltage, as in the other boost converter case. The interleaved single-stage electronic ballast is presented in [8] with two boost inductors and two additional dc-bus capacitors to achieve the high power factor. These ballasts operate at high efficiency around 90%, high power factor 0.97 to 0.99 and low THD between 5 to 10 %; and satisfy the standards mentioned in [9] and [10]. In [11], a new dynamic high frequency model applied to fluorescent lamps is introduced.

In [12], to obtain the high power factor, the HF voltage of constant magnitude is fed in a series with the boost inductor after the rectifier. This improves its efficiency (91%) and power factor (0.99), and THD (below 15%). All these ballasts use large input LC filter (L_f >1mH, C_f >220μF). The coupling inductor is used as the boost inductor in [13] with current injection through the capacitors, which has improved its overall performance

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with efficiency 90%, power factor 0.999 and THD 5%. This paper presents electronic ballast with a new power factor correction circuit combined with the symmetrical half-bridge parallel loaded series resonant inverter topology [14]. The proposed PFC circuit inductor injects its stored energy to the dc-bus capacitors and also feeds the part of the switch current back to the ac input source. The coupling inductor is inserted in series at the output of the rectifier to block the HF ripples. The coils of the coupling inductor carry unequal currents. The differential current flowing through the magnetizing inductance of the coupling inductor induces the emf in the coils. It varies with the instantaneous value of input ac voltage. This HF modulated induced emf always boosts the dc-bus voltage at a required value above the peak of ac input voltage. It is similar to HF voltage injected in series after the rectifier as in [12], but it is unmodulated. The magnetizing and current injecting inductors of the proposed topology carry the bi-directional current in a switching cycle. Therefore, the problem of saturation of magnetic components is avoided. Hence, the position of coupling inductor before or after the rectifier does not affect its performance. The coupling inductor will increase the cost, but it will be compensated over a period of time owing to increased efficiency, UPF and low THD. This coupling inductor is used in place of a three-winding transformer in [12].

The proposed circuit has added advantages. It is suitable for high voltage ac mains above 110 V, because the dc-bus voltage is required to be maintained just above the peak of input ac voltage. It takes ripple free input current with low THD (less than 5%) due to equal switch voltages and currents in a switching cycle, HF frequency current injection and HF modulated voltage. It also maintains the unity power factor and high efficiency even with large changes in input voltage under the worst regulation condition. It requires comparatively less magnetizing inductance (1.44 mH).

The principle of operation, analysis and design procedure of proposed EB is described in section-2. Laboratory prototype electronic ballast is designed for two series-connected (2 x 36W) fluorescent lamps and its experimental results are presented in the subsequent sections. Simulation of the circuit is also carried out to get insight of the circuit behavior.

2. Principle of Operation and Analysis

The first stage of the proposed electronic ballast as shown in Fig.1 consists of a HF full wave bridge rectifier (diodes D_1-D_4) and PFC circuit (C_1, C_2, L_j and L_c), commonly shared MOSFETs S_1 and S_2 plus dc-bus capacitors C_{d1} and C_{d2}. The high value resistances R_1 and R_2 of 470 kΩ connected across the C_{d1} and C_{d2}, forming static equalizing circuits, are used to nullify the effect of deviation in C_{d1} and C_{d2}. During every switching half cycle, the switched inductor L_j injects the current to the dc-bus capacitors C_{d1} and C_{d2}. The capacitors C_1 and C_2 act as the filters for the inductor current i_{Lj}. The part of the switch current is fed-back through L_j at the input of the diode bridge rectifier in the same switching half cycle. The coupling inductor L_c has two identical windings placed on the common core.

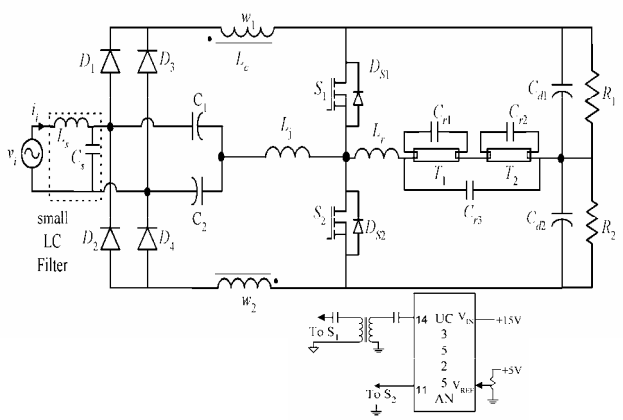

Fig. 1 Circuit diagram of proposed electronic ballast for two series connected fluorescent lamps

As shown in Fig. 2 of the equivalent circuit diagram, it is represented as a transformer with two ideal windings w_1 and w_2, and magnetizing inductance L_m. Both ideal windings carry the same current ($i_{w1} = i_{w2}$) but in opposite directions. The L_m can be referred to either side of L_c. This L_m carries the differential current i_m of both windings and induces the HF voltage v_m across them. The v_m has a frequency equal to twice the switching frequency. The magnitude of v_m changes with the instantaneous value of the input ac voltage. The v_m boosts and maintains the dc-bus voltage at constant value above the peak of ac voltage over the ac input cycle. Therefore, due to the HF current

injection to the dc-bus capacitors and the HF induced emf between the input ac voltage and the dc-bus voltage, the diodes D_1 to D_4 conduct also near the valley of ac line voltage. Thus, the proposed PFC circuit maintains the UPF and low THD of the ac input current.

The second stage consists of MOSFETs S_1 and S_2, dc capacitors C_{d1} and C_{d2}, resonant components L_r and C_{r1} to C_{r3}, and two series connected fluorescent lamps T_1 and T_2. The square-voltage of magnitude $\pm V_d$ /2 at switching frequency (f_s) is fed to the resonant tank circuit, which shape the square wave voltage into a sinusoidal form. The impedance Z_L represents the equivalent load on the inverter. The block diagram of generating PWM gating pulses for switches S_1 and S_2 using IC UC3525AN is shown in Fig. 1.

Under a steady state condition, it is assumed that:

- All the components are ideal.
- The dc-link capacitors C_{d1} and C_{d2} are equal and large enough to be considered as a ripple free voltage source of voltage V_d /2.
- The dc-link voltage V_d is constant and always greater than the peak value of the ac input line voltage v_i, ($V_d > V_p$).
- The input voltage v_i is constant during a switching cycle, since the switching frequency f_s is much greater than the input supply frequency f.
- The inequality in gain between MOSFETs (S_1 and S_2) is always present, the higher gain device turns-on first, and the gate drive for the continuing oscillation comes from the positive feedback.

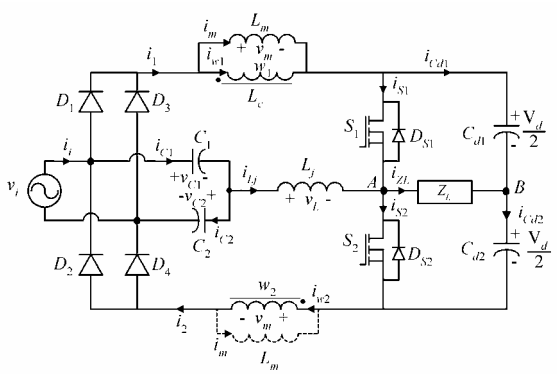

Fig. 2 Equivalent circuit diagram of proposed electronic ballast

This oscillation is reduced to some extent by using ferrite beads and 22Ω resistance at the gate of MOSFETs. The MOSFETs are switched symmetrically with duty ratio (d = 0.5); therefore, the sufficiently large capacitors C_1 and C_2 hold the voltages constant and share the current i_{Lj} equally during the switching period as,

$$v_{C1} = v_{C2} = 0.5\, v_i, \text{ and } i_{C1} = -\, i_{C2} = i_{Lj} / 2 \tag{1}$$

The fluorescent lamps operating at HF are considered as a resistive load [4] of value R_{FL}.

2.1 Operating modes

The operation of the proposed circuit is explained in general detail with the help of six modes shown in Fig. 3 and its simulated waveforms in Fig. 4 in one switching time period T_s. Since the switch capacitances are of small values, the transition period of MOSFETs compared to switching period T_s is negligible. Therefore, the transition of switches is assumed instantaneous and hence, the corresponding modes are not included. Prior to mode 1, the inductor currents i_{Lj} and i_m are at their peak values $+I_{Lj}$ and $-I_{Lj}$ respectively and flowing through the S_2, L_m, D_4, v_i, C_1, C_2 and L_j. The dc-bus capacitor C_{d2} is supplying the current i_{ZL} at its negative peak value $-I_{ZL}$ through S_2.

Mode 1 [t_o - t_1], Fig. 3(a): At t_o, the switch S_2 is turned off. The diodes D_{s1} and D_1 turn on. The inductor L_j starts injecting its stored energy to the dc-link capacitors C_{d1} and C_{d2} through D_{s1} via L_c, D_4, v_i, C_1, and C_2. The capacitors C_{d1} and C_{d2} also receive energy from the input mains. The inductance L_m starts storing the energy from the input ac mains. The inverter load current i_{ZL} freewheels through the D_{S1} and C_{d1}. During this mode,

$$v_m = -\left(V_d - v_i\right)/2 \tag{2}$$

$$v_{Lj} = v_m - v_{C1} \tag{3}$$

From (1) – (3), $v_{Lj} = -\, V_d / 2$ (4)

The inductor current i_{Lj} decreases linearly from $+I_{Lj}$ as,

$$i_{Lj}(t) = I_{Lj} - \frac{V_d}{2L_j}(t - t_0) \tag{5}$$

$$i_m = -\,i_{Lj},\ i_{ZL} = i_{Cd1} - i_{Cd2},\ ,\ i_i = i_1 + \frac{i_{Lj}}{2} = i_2 - \frac{i_{Lj}}{2} \qquad (6)$$

At t_1, i_{Lj} decreases to zero, since the injection of energy is over. The load current i_{ZL} becomes zero. Therefore the diode D_{s1} turns off. The current i_m and i_{Cd1} also become zero, since the energy storing in L_m and C_{d1} is completed.

Mode 2 [t_1 - t_2], Fig. 3(b): At t_1, switch S_1 turns on. Thus ZVS of S_1 is achieved. The inductor L_j starts restoring energy from the inductor L_m through switch S_1. Therefore, the currents i_{Lj} and i_m vary linearly at the same rate as mode 1, but in an opposite direction. The capacitor C_{d1}, along with ac mains, starts supplying its energy to the inverter load Z_L. At the end of this mode, at t_2, the currents i_{Lj} and i_m reach their peak values $-I_{Lj}$ and $+I_{Lj}$ respectively.

During above modes 1 and 2, the current i_1 increases linearly from 0 to I_{Lj}; whereas, the current i_2 decreases linearly from I_{Lj} to 0. Therefore, the instantaneous average value of input current during t_0 - t_2, as per (6), is the sum of the average value of i_1 and $i_{Lj}/2$,

$$i_{iav} = i_{1av} + (i_{Lj}/2)_{av} = I_{Lj}/2 + 0 = I_{Lj}/2 \qquad (7)$$

Mode 3 [t_2 - t_3], Fig. 3(c): At t_2, the capacitor current i_{Cd2} becomes zero. Therefore, the diode D_4 turns off. During this mode, the L_m returns its remaining energy, as the $L_m > L_j$, to the ac mains through L_j via S_1, C_1, C_2 and D_1. The currents i_{Lj} and i_m clamp at corresponding peak values, since the inductor L_j has stored the full energy. Therefore,

$$v_{Lj}(t) = 0\ ,\ v_m(t) = v_{C1} = 0.5v_i \qquad (8)$$

The input current is, $i_i = +\,I_{Lj}/2$ (9)

The capacitor C_{d1} continues to supply energy to the Z_L until t_3.

Mode 4 [$t_3 - t_4$], Fig. 3(d): At t_3, the upper switch S_1 is turned off. The diodes D_{s2} and D_4 turn on. In this mode, the inductor L_j injects its stored energy to the dc-link capacitors C_{d1} and C_{d2} through D_{s2} via C_1, C_2, v_i, D_1, and L_c. The L_m, C_{d1} and C_{d2} store the energy from the ac mains. The current i_{ZL} freewheels through the C_{d2} and D_{S2}.

During this mode,

$$v_m = -(V_d - v_i)/2 \qquad (10)$$

$$v_{Lj} = v_{C2} - v_m \qquad (11)$$

From (1), (10) and (11), $v_{Lj} = V_d/2$ (12)

The inductor current i_{Lj} increases linearly from $-I_{Lj}$ as,

$$i_{Lj}(t) = -I_{Lj} + \frac{V_d}{2L_j}(t - t_3) \qquad (13)$$

$$i_m = -\,i_{Lj},\ i_{ZL} = i_{Cd2} - i_{Cd1},\ i_i = i_1 + \frac{i_{Lj}}{2} = i_2 - \frac{i_{Lj}}{2} \qquad (14)$$

This mode continues until the energy of L_j is exhausted and the energy storing in L_m is over, that is up to t_4.

Mode 5 [$t_4 - t_5$] Fig. 3(e): At t_4, the currents i_{Lj} and i_{ZL} become zero; therefore, the diode D_{s2} turns off and the lower switch S_2 turns on. Thus ZVS of S_2 is achieved. The inductor L_j starts receiving its energy from L_m through S_2. The currents i_{Lj} and i_m continue to vary linearly at the same rate as in the last mode but in an opposite direction. During this mode, dc-link capacitor C_{d2} supplies its energy to the load Z_L along with ac input source. At the end of this mode i.e. at t_5, the currents i_{Lj} and i_m reach their peak values $+I_{Lj}$ and $-\,I_{Lj}$ respectively, as the L_j has restored its energy to full capacity.

During above modes 4 and 5, the current i_2 increases linearly from 0 to I_{Lj}; whereas, the current i_2 decreases linearly from I_{Lj} to 0. Therefore, the instantaneous average value of input current during $t_3 - t_5$, as per (14), is the sum of the average value of i_1 and $i_{Lj}/2$,

$$i_{iav} = i_{1av} + (i_{Lj}/2)_{av} = I_{Lj}/2 + 0 = I_{Lj}/2 \qquad (15)$$

Mode 6 [$t_5 - t_6$], Fig. 3(f): The capacitor current i_{Cd1} becomes zero at t_5. Therefore, the diode D_1 turns off. During this mode, the L_m returns its remaining energy to the ac mains through L_j, via S_2,C_1,C_2 and D_4. The currents i_{Lj} and i_m clamp at their corresponding peak values, as in mode 3. The capacitor C_{d2} continues to supply the energy to load Z_L. This mode ends at t_6, when the gate pulses applied to the MOSFETs are inverted. This instant also completes the operation of one switching cycle. During this mode,

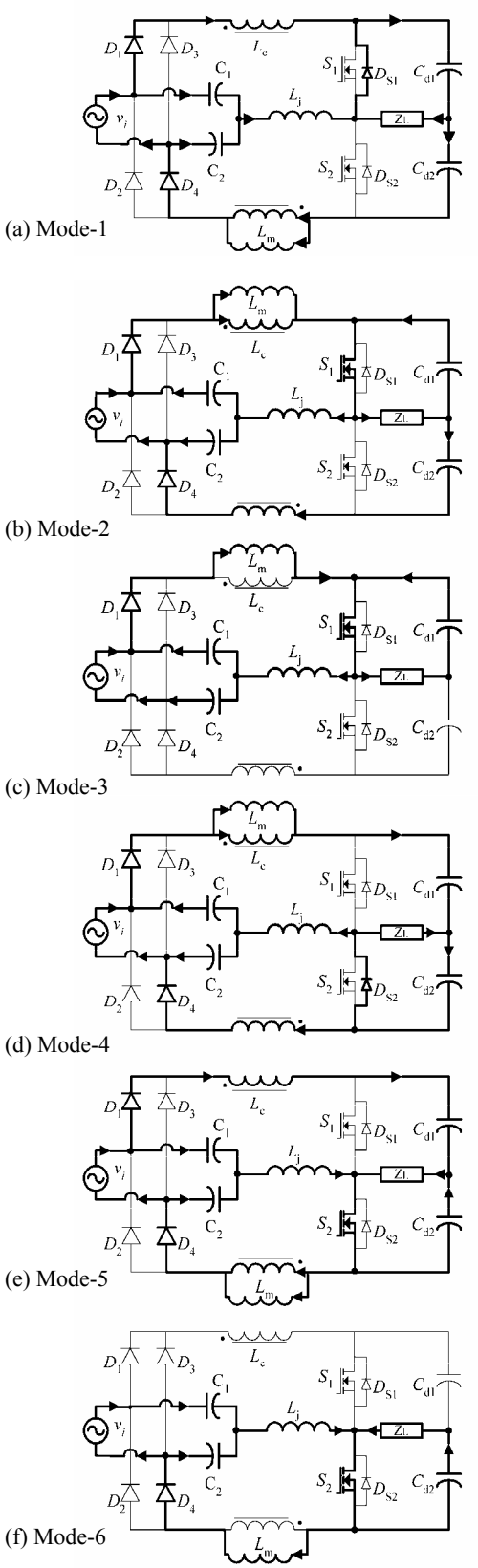

Fig. 3 Operating modes of PFC and inverter output circuits

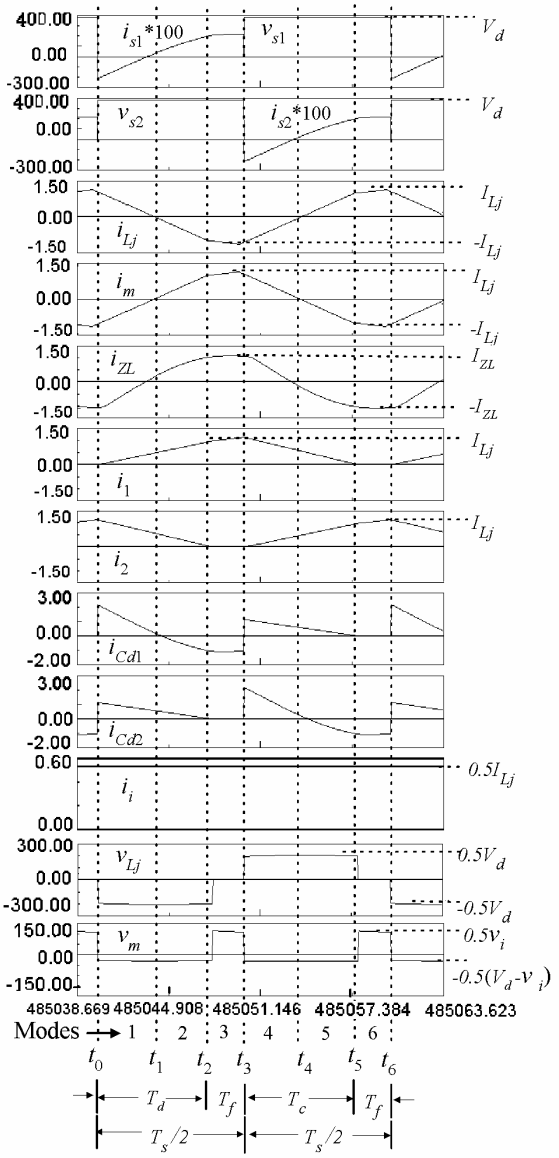

Fig. 4. Simulated waveforms of PFC circuit in electronic ballast.

$$v_{Lj}(t) = 0, \quad v_m(t) = v_{C2} = 0.5v_i \tag{16}$$

$$\text{and} \quad i_i = +I_{Lj}/2 \tag{17}$$

2.2 Analysis of PFC circuit

From the previous discussion, it is evident that,

(i) In each switching half cycle, the switched inductor L_j injects the current to the dc-bus capacitors.

(ii) At every instant, the inductance L_m of L_c carries the equal and opposite current of L_j, $i_{Lj} = -i_m$. These currents

vary linearly from positive to negative peak values or vice-versa in every switching half cycle at a rate twice that for boost inductor current in other unconventional PFC circuits [12].

(iii) The HF induced emf v_m in L_c is a modulated one and its magnitude varies with the instantaneous value of input voltage over the supply cycle. Its frequency is twice the switching frequency. The v_m boosts and maintains the dc-bus voltage at a constant value V_d, above the peak of input ac voltage, over its complete cycle.

(iv) Over the switching cycle, the input current i_i is constant and equal to half of the peak value of switched inductor current, $i_i = I_{Lj}/2$.

Therefore, the power factor and THD of this proposed circuit are better than other circuits; and a very small *L-C* filter is required at the input to get the ripple-free current.

Considering the time period of linearly decreasing and increasing current i_{Lj} as $T_d = (t_2 - t_0)$ and $T_c = (t_5 - t_3)$ respectively, and applying the equal area criteria to the curves of v_{Lj} and v_m of Fig. 4,

$0.5V_dT_d = 0.5V_dT_c$, and

$$0.5(V_d - v_i)(T_d + T_c) = 0.5v_i(0.5T_s - T_d) + 0.5v_i(0.5T_s - T_c)$$

By solving above equations, the time period of linearly varying current is,

$$T_l = T_d = T_c = \frac{v_i}{V_d}\frac{T_s}{2} \tag{18}$$

At $T_l/2$, the inductor current i_{Lj} given by (5) and (13) is zero. Therefore the peak value of i_{Lj} is,

$$I_{Lj} = \frac{T_s v_i}{8L_j} \tag{19}$$

Where, v_i is the instantaneous value of ac input voltage during that switching cycle and given as

$$v_i = V_p \sin \omega t \tag{20}$$

Therefore, the input current i_i remains constant at $i_i = \frac{T_s v_i}{16L_j}$ during the corresponding switching cycle, and varies in-phase with the input voltage v_i over the input supply cycle as,

$$i_i = I_p \sin \omega t, \quad I_p = T_s V_p / 16L_j \tag{21}$$

The input power to the ballast is,

$$P_i = \frac{1}{2\pi}\int_0^{2\pi} v_i i_i \, d\omega t = T_s {V_p}^2 / 32L_j = T_s V^2 / 16L_j \tag{22}$$

Where, V is the rms input line voltage.

From (20) – (22), it is evident that the input current follows the ac mains voltage i.e. the proposed ballast topology operates at UPF.

The switched inductor is calculated as,

$$L_j = T_s {V_p}^2 / 32P_i = T_s V^2 / 16P_i \tag{23}$$

The input power (P_i) can be calculated from output power (P_o) of ballast and by assuming expected efficiency (η) as,

$$P_i = P_0 / \eta \tag{24}$$

2.3 Magnetizing inductance L_m and dc-bus voltage V_d

The inductances L_m and L_j carry the flat top current of value I_{Lj} during the modes 3 and 6, $T_f = \frac{T_s}{2} - T_l = \frac{T_s}{2}\left(1 - \frac{v_i}{V_d}\right)$, which varies with the instantaneous input voltage v_i over the half cycle of ac mains. T_f varies from maximum $T_s/2$ (ideally) at the valley point of pulsating rectified ac input to minimum zero (ideally) at its peak. Therefore, the minimum value of L_m is calculated as follows,

$$L_{m\min} = \frac{v_{m\max} T_s}{2 I_{Lj}} \tag{25}$$

From equations (8), (16), (19) and (25);

$$L_{m\min} = 2L_j \tag{26}$$

That is to maintain dc-bus voltage V_d above the peak value of ac input voltage (at duty ratio 0.5), L_m should be greater than $2L_j$. Therefore,

$$V_d = \frac{L_m}{2L_j} V_p \tag{27}$$

From the above equations, the input stage of the proposed ballast always operates as a boost converter, since the voltage V_d is always above the peak voltage V_p

over the complete ac input cycle [12]. This is ensured by an appropriate value of L_m greater than twice L_j.

2.4 Calculations of PFC and inverter circuit components

Specification of the ballast

Input voltage, V = 230 V, 50 Hz

Operating voltage range = 180 ~ 260 V

Rating of fluorescent lamps, P_0 = 2 x 36 = 72 W

Switching frequency, f_s = 50 kHz.

The design of PFC components including magnetizing inductance (L_m) is very crucial to operate the ballast at UPF, high efficiency with low THD.

From (23) and (24), L_j = 0.854 mH with 93 % efficiency, but to operate the ballast at UPF over the operating range with sufficient light intensity, the value of L_j should be less than calculated above, therefore it is selected as 0.65 mH. The capacitors C_1 and C_2 are fixed at 0.1 μF (polypropylene).

Assuming the dc-bus voltage 10% above the input peak voltage (i.e. above 325V for 230V rated input voltage), V_d =360 V; from (27), L_m = 1.44 mH.

Generally, for a single-phase application, the boost converter is recommended as an HPF rectifier, due to its simple circuitry and the current-source characteristic verified in its input. However, it is important to observe that the boost converter is operational only in the voltage step-up mode, which means that the dc-bus voltage must be higher than the peak value of the voltage provided by the ac supply system. Therefore, the dc-bus voltage must be always higher than the corresponding input peak voltage by 10%. The DC link capacitors C_{d1} and C_{d2} are selected as = 22 μF (electrolytic).

By adopting the procedure in [1,15] and [16] for discontinuous current mode, the parameters of the inverter circuit are,

$$L_r = 1.36 \text{ mH}, C_{r1} = C_{r2} = 10\,nf, C_{r3} = 5\,nf,\ f_0 = 43 \text{ kHz},$$
$$V_{FLs(peak)} = 300 \text{ V},\ I_{FLs(peak)} = 0.48 \text{ A},\ R_{FLs} = 625\ \Omega,$$
$$Z_0 = 369\,\Omega, (V_d / V_{FLs}) = 1.2, (f_s / f_0) = 1.16 \text{ and } Q = 1.7$$

Diodes: UF5408 and MOSFETs: IRF 840 are selected on the basis of peak currents. The small input filter with L_s =50 μH and C_s=0.01 μF is used.

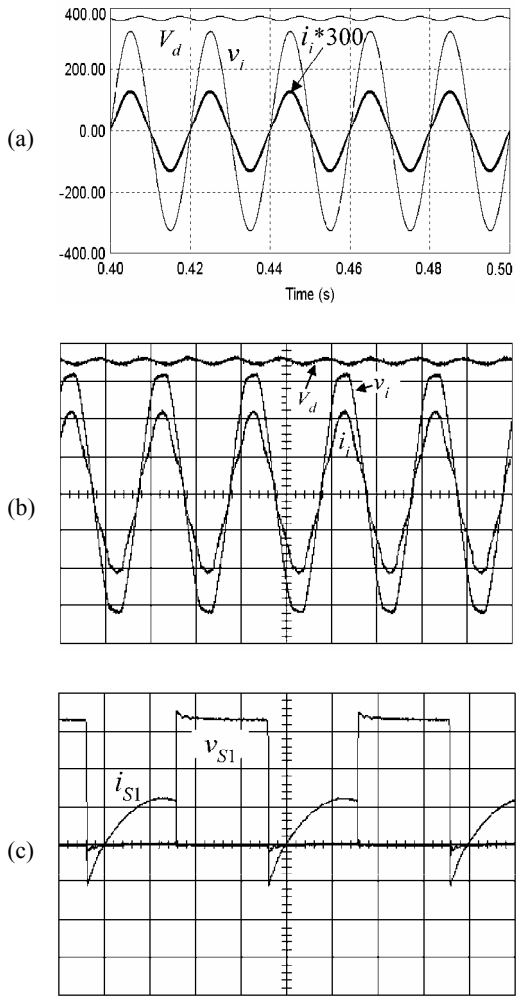

Fig. 5 Simulated and experimental results: (a) simulated waveforms of dc-Link voltage (V_d), input voltage (v_i) and input current (i_i); (b) experimental waveforms of dc-Link voltage (V_d), input voltage (v_i = 230 V) and input current (i_i): (100 V/div, 0.2 A/div, 10 *m*s/div) and (c) experimental switch voltages (v_{S1}) and switch currents (i_{S1}): 100 V/div, 1 A/div, 10 μs/div)

3. Experimental Results

The laboratory prototype of the proposed electronic ballast is built and tested. The PWM IC UC3525AN is used to generate the gate pulses. The switching frequency is kept above the resonant frequency. Therefore, circuit behavior is inductive. This limits the inrush current through the circuit. By using the inbuilt soft-start, the duty ratio is changed automatically from low to 0.5, which

provides the preheating current to the filaments of FLs. This also helps in limiting the inrush current. The experimental results are obtained with variations in input voltage from 180 to 260 V at switching frequency 50 kHz and duty ratio 0.5. The effect of the PFC circuit can be seen in Fig. 5(a) and (b). The dc link voltage (V_d =360 V) is above the peak value (V_p =325 V) for input ac voltage at 230V rms. In the proposed topology, the dc-bus voltage remains below 400V for the 230V utility supply. Thus the voltage rating of the MOSFETS does not have an appreciable effect. The experimental results shown in Fig. 5(b) are matching with the simulated results shown in Fig. 5(a).

Fig. 5(c) shows the ZVS operation of the switches. The experimental waveforms of input line voltage (v_i) and current (i_i) at various values of input voltage in the operating range are shown in Fig. 6 and it is evident that the proposed ballast maintains UPF over a wider input voltage range.

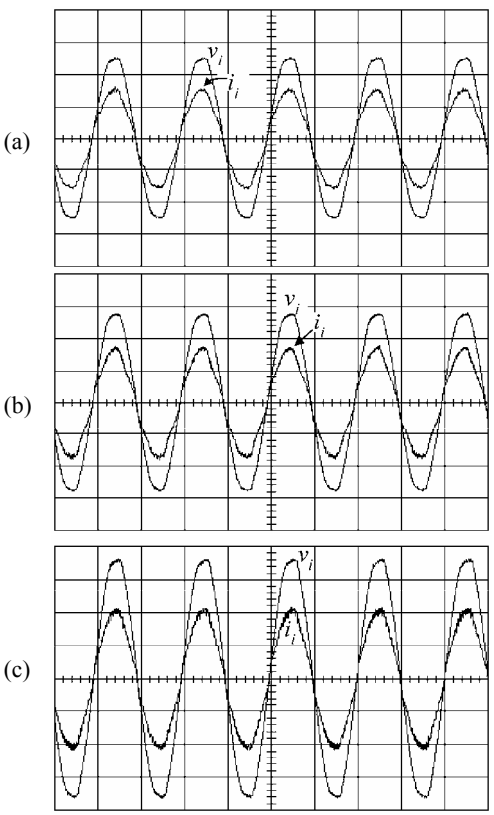

Fig. 6 Experimental waveforms of input voltage (vi) and current (ii) at (a) 180 V, (b) 210 V, (c) 260 V (100 V/div, 0.2 A/div, 10 ms/div)

The output waveforms of the HF fluorescent lamp voltage (v_{FL}) and current (i_{FL}) are given in Fig. 7(a). The experimental envelope waveform of lamp current shown in Fig. 7(b) is flat. The crest factor of the lamp current experimentally found is 1.39. It can be seen that these waveforms are nearly sinusoidal in nature with minimum ripple, which prolongs the lifetime of the fluorescent lamps. The experimentally obtained performance parameters of electronic ballast are shown in Fig. 8, which shows that the power factor is maintained at unity, efficiency between 93.8 – 94.2% and the THD less than 3.2 % over the operating voltage range.

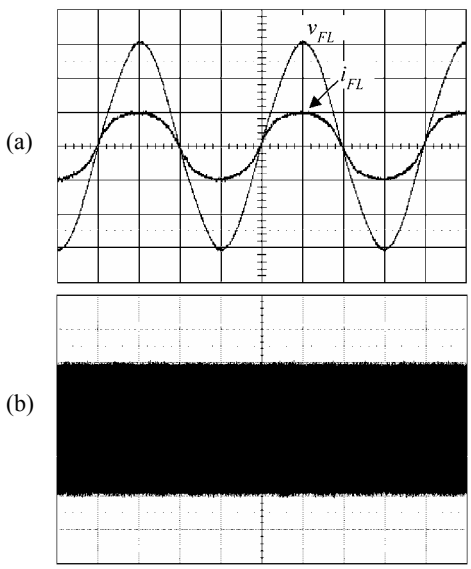

Fig. 7 Experimental results: (a) fluorescent lamp voltage (v_{FL}) and current (i_{FL}) at input voltage (v_i) 230 V: (100 V/div, 0.4 A/div, 10 μs/div), (b) envelope of lamp current (i_{FL}): (0.2 A/div, 10 ms/div)

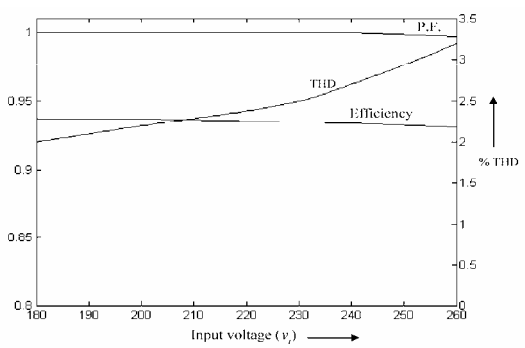

Fig. 8 Experimental Input power factor, Efficiency, and %THD

4. Conclusion

In this paper, the single-stage electronic ballast based on the current injection technique is proposed. Its principle of operation, theoretical analysis and design procedure of the proposed EB have been presented.

Due to injection of HF current to the dc-link capacitors and the HF modulated induced emf of the coupling inductor, the proposed circuit maintains the UPF with low THD even under wide variation in ac input voltage. In addition, the coupling inductor blocks the high frequency ripples. Therefore, a comparatively small *L*-*C* filter is required at the input of circuit to get the ripple-free input current. The two capacitors used in the injection path serve as the filter and also freewheeling components instead of freewheeling diodes, which increase the reliability. The two smaller value dc-link capacitors are required compared to a single large capacitor and no additional blocking capacitor is required.

The laboratory prototype of the proposed circuit is built for (2x36W) series-connected fluorescent lamps operating at 50 kHz and 230V line voltage. For series connected fluorescent lamps as in [1], the current through the switches reduces, which results in reduction of conduction losses. However, the proposed topology can be used for parallel-connected fluorescent lamps or a single lamp with slight modifications in tank circuit. The proposed single-stage electronic ballast has UPF, low THD and high efficiency. The proposed EB can be used with an output HF transformer without affecting the performance. The use of the transformer ensures the proper galvanic isolation of the fluorescent lamps.

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